Strained Si for Sub-100 nm MOSFETs

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The basic idea in strained Si CMOS is to modify the carrier transport properties of Si by introducing strain in order to improve performance of MOSFETs. The biaxial tensile strain in the strained Si layer on relaxed SiGe can be tailored by the Ge content. For instance, ~1.2% strain is obtained in Si pseudomorphically grown on fully relaxed SiGe with 30% [Ge]. Band offsets at the Si/SiGe interface, smaller bandgap and change in dopant diffusivity in SiGe require re-centering of device characteristics. Short channel strained Si NFETs with proper V_T and C_{ov} design have been demonstrated in a 0.13 μm bulk CMOS technology [1]. For NFETs, current drive enhancement of 15~20% was observed in devices with mild amount of strain (13% [Ge]). Using higher amount of strain (28% [Ge]), 7~10% increase in PFET current drive was also observed [1]. A novel electrical characterization technique was used to show that low field mobility enhancement is retained even in sub-100 nm channel lengths in spite of significantly higher channel doping concentration required (Fig. 1) [2].

Larger and more symmetric enhancements of electron and hole mobilities require higher amount of strain. NFET mobility increases with strain by as much as 110%, with the enhancement beginning to saturate at higher strain (ε>1.3%) (Fig. 2). On the other hand, PFET mobility initially exhibits a slight degradation at low amount of tensile strain, but increases linearly with higher strain (Fig. 3). The trade-off between mobility enhancement and difficulty in maintaining high material quality is a critical challenge in realizing strained Si ULSI technology. This point is illustrated in Fig. 4 where electron and hole mobility enhancement is plotted against thermodynamic critical thickness, estimated by that calculated for pseudomorphic SiGe on Si [3].

Strained Si MOSFETs have been demonstrated on SiGe-on-insulator (SGOI) substrates prepared by several techniques ([4] and [5] for example), and sub-100 nm devices with significant current drive enhancement have recently been demonstrated on ultra-thin thermally-mixed SGOI (TM-SGOI) with sub-nanometer surface roughness (Fig. 5) [5]. Short channel devices were also fabricated on bonded SGOI (BSGOI) created by the layer-transfer technique (Fig. 6) [6]. An epitaxially grown relaxed SiGe layer was transferred to a handle wafer by wafer bonding and the SmartCut process. The strained Si channel layer was epitaxially grown on the transferred layer. Excellent V_T roll-off characteristics have been observed in gate lengths down to sub-50 nm regime (Fig. 7). When self-heating is reduced in both BSGOI and SOI control devices by pulse measurements (Fig. 8), BSGOI NFETs result in current drive enhancements that are comparable to those observed in bulk strained Si devices [1]. BSGOI approach utilizes well-studied relaxed SiGe buffer layer, but the manufacturability of the SiGe layer transfer technique is a critical challenge. The device integration demonstrations in TM-SGOI and BSGOI represent progress towards realizing the combination of the high mobility in strained Si and advantages of SOI structures in aggressively scaled device dimension.

The layer transfer technique can be extended to fabricate ultra-thin strained Si-directly-on-insulator (SSDOI) structures. Fig. 9 shows the XTEM of a sub-10 nm strained Si layer directly on oxide. The structure was fabricated by layer-transferring a strained Si/relaxed SiGe hetero-layer, and by selectively removing SiGe, leaving strained Si directly on the oxide. Similar approaches have recently been reported [7, 8]. Since the

thickness of the SSOI is determined by the epitaxial process and the selective removal of SiGe, (as opposed to CMP and sacrificial oxidation steps) excellent thickness and uniformity control can be expected. Raman spectroscopy (Fig. 10) confirmed that the tensile strain in the Si layer was retained in the final structure, even after thermal annealing for 7.5 minutes at 1000°C. Such SSOI structures are promising for applications in single and double gate devices with ultra-thin strained Si channel.

References

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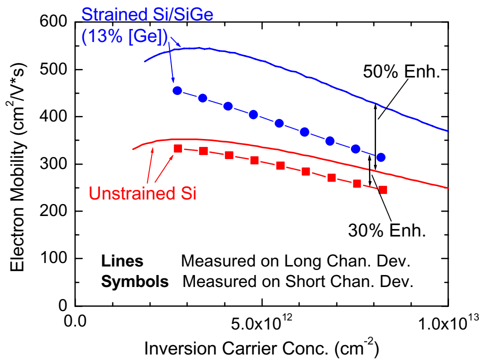

Fig. 1 Comparison of mobility in strained and unstrained Si devices. Mobility is extracted by the *dR/dL* method in short channel devices [2].

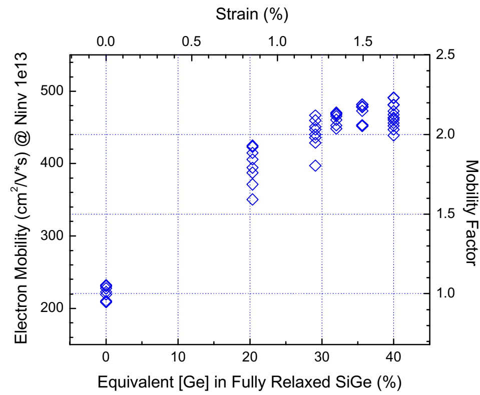

Fig. 2 NFET mobility at N_{inv} = 1e13 cm^{-2} as a function of strain. Electron mobility enhancement saturates at higher strain (ε>1.3%).

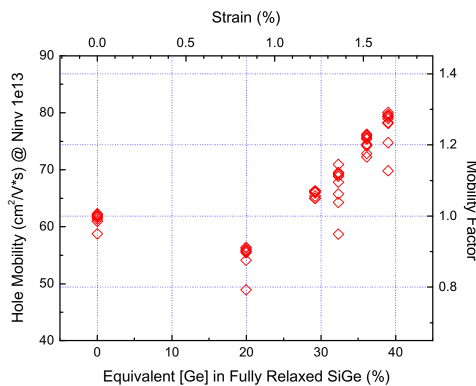

Fig. 3 PFET mobility at N_{inv} = 1e13 cm^{-2} as a function of strain. Sizable hole mobility enhancement requires high strain (ε>1.3%).

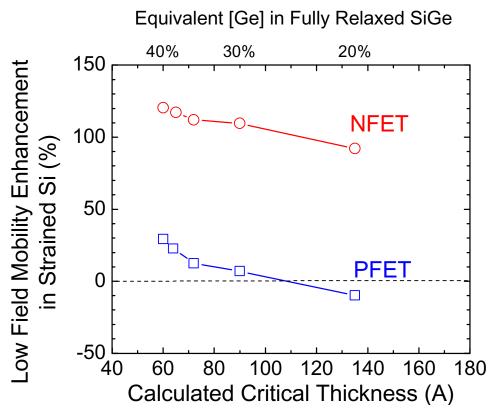

Fig. 4 Trade-off relationship between inversion mobility enhancement and theoretically calculated critical thickness from Matthews & Blakeslee (J. Cryst. Growth, vol 27, p. 118, 1974.)

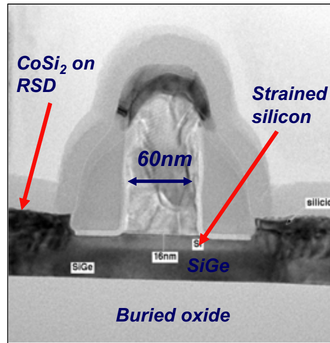

Fig. 5 TEM micrograph of a strained Si MOSFET fabricated on ultra-thin thermally mixed SGOI (TM-SGOI) [5].

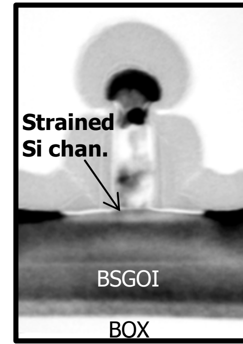

Fig. 6 TEM micrograph of a strained Si MOSFET fabricated on bonded SGOI (BSGOI).

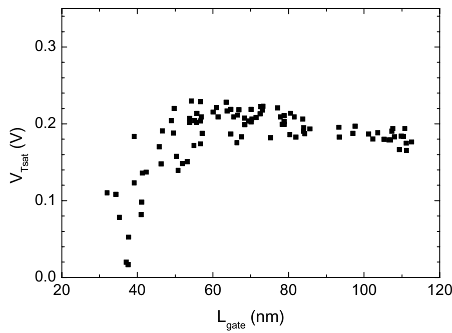

Fig. 7 V_T roll-off characteristics of NFETs fabricated on BSGOI. Excellent control of SCE is observed down to sub-50 nm gate lengths.

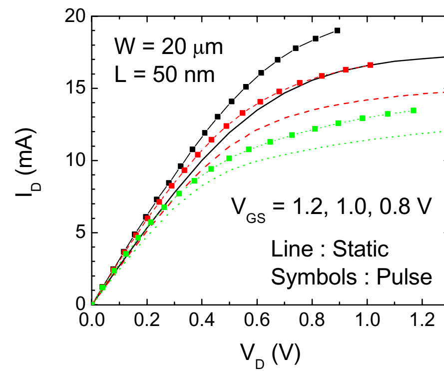

Fig. 8 Output characteristics of a NFET fabricated on BSGOI. Significant self-heating is observed during static DC operation as evidenced by the difference between the pulse and static measurements.

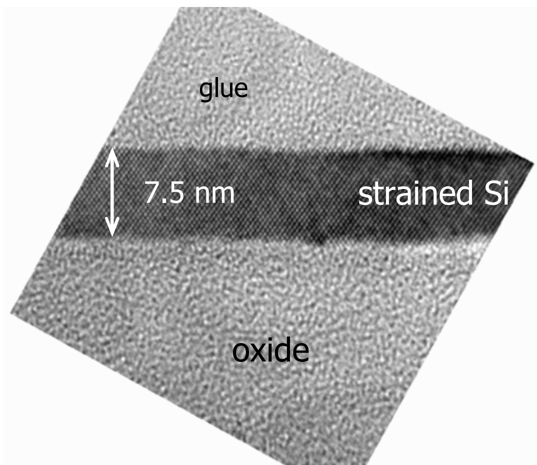

Fig. 9 HR TEM micrograph of a 7.5 nm-thick strained Si layer directly on oxide.

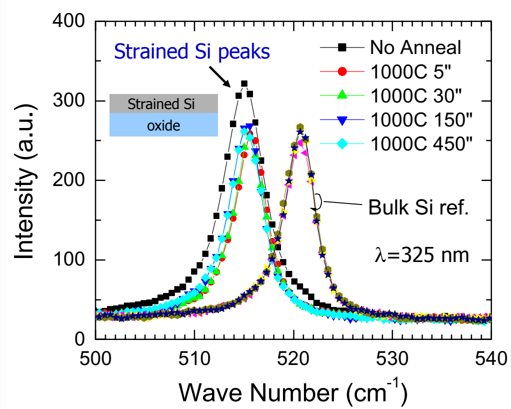

Fig. 10 Raman spectrum of strained Si directly on oxide. Strained Si peaks do not shift even after 7.5 minutes of annealing at 1000°C, indicating that strain was retained during thermal annealing.