Low Open Area Logic 130 nm Contact Etch Endpoint

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Logic circuit devices are characterized by the critical dimension of their gate electrode. This is minimized in order to increase their operating frequency. The complex wiring of logic-circuit chips, requires multiple levels of metallization, placing increased emphasis on "back-end-of-line" (BEOL) oxide and/or metal etching.

The contact dry etch process (CA process) is a critical step in the fabrication of 130 nm logic devices since the main risk is to obtain an open contact. These leading edge products present critical structure dimensions of 0.18 - 0.13 μm with copper backend.
The four main challenges in CA etch process monitoring are:

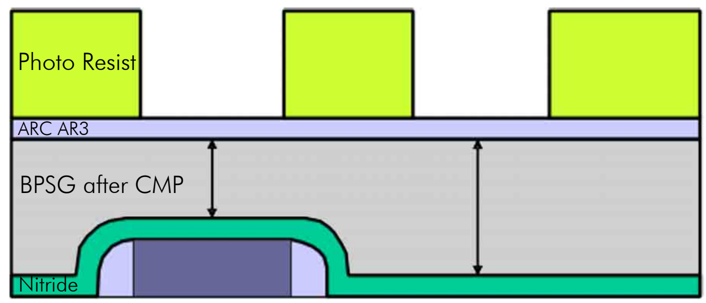
- Low open area oxide, less than 2%
- Highly selective fluorine process
- Rotating magnetic field employed in the etch tool
- Two types of contacts (pad and floating gate) have to be etched at the same time

Such difficult process can be controlled using the industry standard end point detection by CCD - optical emission spectroscopy method. The PlasmaScope from HORIBA Jobin Yvon is a powerful plasma monitoring system that demonstrates advanced capabilities to provide accurate and stable end point detection in CA etch process. The OES endpoint solution proves to be ready for production whatever technology and product and is implemented in-line to ensure a reliable process control in the CA etch step.

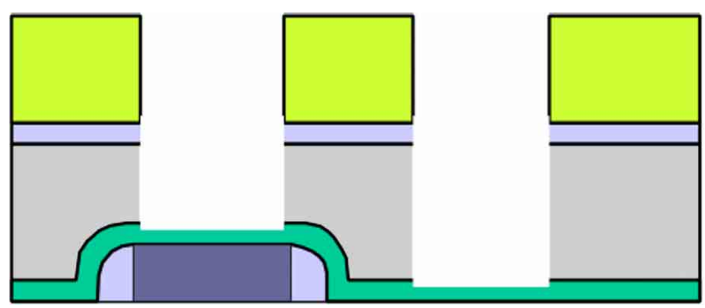
Experimental

Processing is performed in a TEL DRM etch tool that integrates a magnetically enhanced RIE system (MERIE).

The HORIBA Jobin Yvon PlasmaScope was used to collect the plasma emission during the CA etching process. This portable system is equipped with a sturdy optical fiber which can be easily mounted on the side window of the plasma chamber. It uses a 2048 CCD sensor designed for multi channel spectroscopy, and covers the spectral range from 190 to 850 nm.
By monitoring the emission intensity of selected wavelengths the PlasmaScope tracks the amount of material in the plasma, and hence whether a particular material has been completely removed from the etch surface. Thus the end point is detected based on the changes in the spectrum of radiation emitted by the plasma.
The wafer structure is composed of four layers. The resist is used as a soft mask. To reduce the degree of substrate reflectivity, an organic antireflective coating (ARC) is utilized. The CA process removes the ARC and BPSG layers down to reach the BPSG/Si_3N_4 interface.



Wafer structure before CA etching



Wafer structure after CA etching

Results

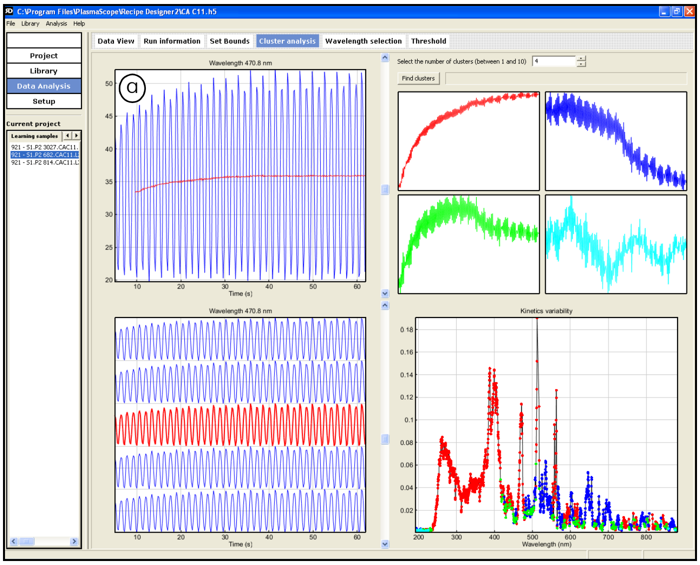
To achieve the implementation of in-line OES system in the CA etch process step three stages were required:

① The selection of the relevant wavelengths that carry the information about the transition

The difficult plasma conditions were overcome by using the advanced AutoPattern software. It automatically analyzes the full spectral data over the complete run and classifies each wavelength according to the shape of its intensity profile. Then it provides the automatic identification of relevant emission lines. For the accurate monitoring of the CA etch process, 20 wavelengths were used by the algorithm.

② Real-time data filtering and the construction of an endpoint indicator

The endpoint recipe can be rapidly constructed to include the wavelengths identified by the AutoPattern software along with advanced signal arithmetic and filtering to remove the effect of the rotating magnetic field.

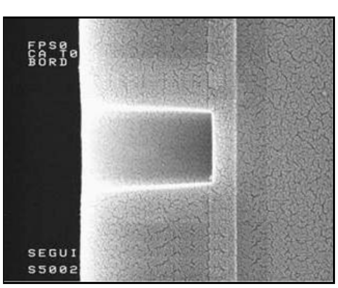


Relevant wavelengths pattern research using Autopattern software
Note the initial raw data showing a very noisy signal on graph a

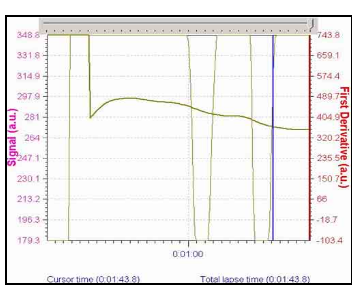
③ A series of tests to expose the algorithm to the reality of production fluctuations

The PlasmaScope measurements were confirmed after the etch using a scanning electron microscope (SEM). SEM pictures exhibit very good agreement with experimental results.

SEM picture and data are provided with the courtesy of ALTIS Semiconductor.

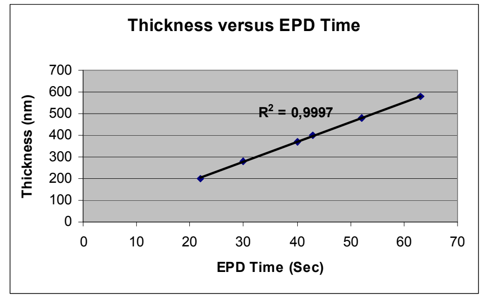


SEM cross section after the CA etch process



Endpoint trace showing the process termination (detection) on floating gate and Pad

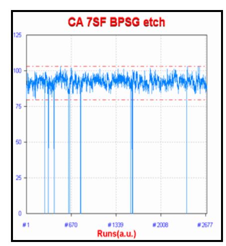
Another test was used to validate the endpoint detection. Several wafers with different BPSG thickness were processed. The figure shows the excellent correlation between the increase of endpoint detection time and the BPSG thickness. It clearly illustrates the PlasmaScope's powerful detection capabilities of the SiN interface.



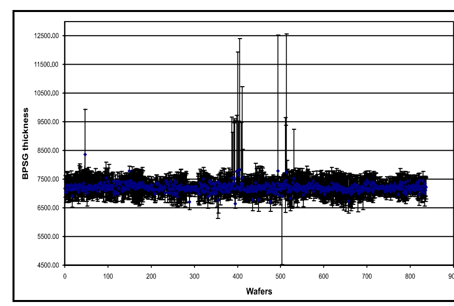
Endpoint algorithm validation

Statistics were performed on 2700 wafers, and 99.7 % successful endpoint detection was achieved.
The end point detection time varied by 18 s which is explained by three factors:

- BPSG deposition after the CMP process,
- Uniformity across and between wafers,
- Variability caused by different open areas from batch to batch.



Statistics on production wafers



BPSG thickness after CMP process

Moreover the PlasmaScope was shown to be production ready by its ability to detect wafer mismatches as no end point was called in the case of blanket resist and double etch wafers.

Conclusion

Monitoring the CA etch process was extremely challenging and the end point detection using OES method proves to be a powerful technique that meets the plasma-etching needs of the next generation of logic chips.
The sensitivity of the system, its multiple wavelength processing and the advanced algorithms included in its software, the PlasmaScope guarantees tight and reliable endpoint detection in the most difficult plasma process conditions.
Moreover the PlasmaScope proves its ability to suit the advanced requirements of high volume production.

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